# ABACOM Technologies

RX-DFM-5V   Digital FM Receiver Module

RX-DFM-5V Frequency Modulation (2FSK) superhet receiver is suitable for use with its companion **TX- DFM-5V** transmitter module. Reception of raw RS232 digital data without the need for any data encoding or decoding is made possible, further simplifying the implementation of an RF link. There are no character or transmission time limitations which exist with other devices . Maximum baud rate of 19200 bit/s and fast start-up time (less than 1 ms).
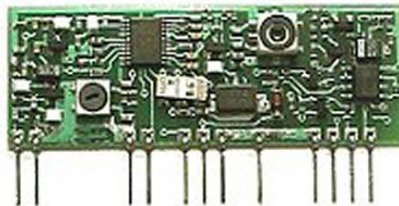

Technical Specifications

- Superhet 2FSK Receiver with single IF conversion from SAW resonator
- Low output logic level (0V) with no modulation
- Start-up time less than 1 ms
- Receiver enable / disable (pin 19) via TTL or CMOS signal: RX Enable = +3 to 5 V
- 5V ±200 mV single supply with consumption lower than 15 mA (13 mA typical)
- High-reliability PCB SIL module
- Dimensions: 54.8 x 22 x 4.5 mm. Pin pitch 2.54 mm.
- Operating frequency : 433.85 MHz + 40 KHz
- RF Input impedance: 50W
- RF sensitivity : -100 dBm
- Baud rate: 2400-19200 baud
- Digital FM detector driven via squelch circuit
- Open collector data output (pin 18) with 5 mA max current
- Squelch threshold externally adjustable from -50 dBm to -100dBm
- Auxiliary output (pin 10) turned On from RX Enable (pin 19): max. current 10mA

Pin Description

PIN	Function
1	RF Input
2,7,12,14,17	Ground
8	Squelch Level
10	Auxiliary Output
11	Carrier Detect
18	Data Output
19	RX Enable (+3V to 5V)
20	+5V Supply

Block diagram
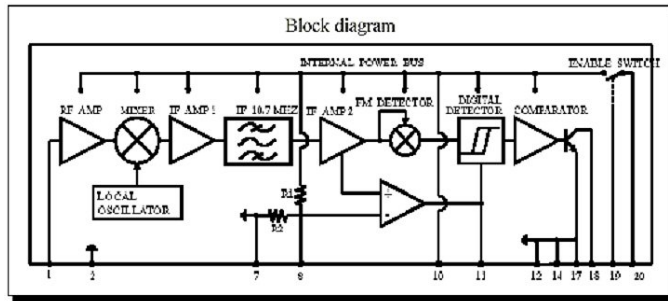
Main Features

- Reception carrier frequency at 433.85 MHz, with 2FSK demodulation and nominal deviation at +40 KHz.
- RF sensitivity: -100dBm.
- Carrier On-Off detector with externally adjustable threshold from -50dBm up to the receiver max sensitivity (-100dBm).
- Bit rate from 2,400 to 19,200 baud with 1 start bit, 8 data bits, 1 stop bit format.
- Direct compatibility with RS232 protocol with no need for intermediate coding and no restriction of symbol and transmission time.
- Data output disabled (0V) when no carrier is present (0V).
- Low output logical level with no modulation.
- Time delay from carrier detection (Carrier Detect output On) to the first correctly detected bit less than 500µsec.
- Time from receiver start-up (RX Enable On) to received data validity less than 1 msec.
- Availability of complete receiver disabling facility (TTL or CMOS logic line) forcing a zero con-sumption state.
- Auxiliary supply output turned on from RX Enable pin: max supply current 10 mA.
- Data output with external push-pull to assure compatibility with different voltages (open collector with a 5 mA max current).
- Single +5V ±200mV Power Supply with less than 15mA consumption (13mA typical).
- ETS 300-200 compatible.

Pin Description

1. **RF input**. A 50Ω impedence antenna is required
2. **Ground.**
7. **Ground.**
8. **Set Squelch Level**. Following schematics show how to connect an external potentiometer to modify the default squelch level. Since pin 8 is at the center of a 100K/6.8K resistor network connected to the supply voltage, the squelch nominal voltage, with no external circuitry, is around 210mV.
10. **Aux Out**. Auxiliary supply output, is available as soon as the receiver goes active. Available to supply external devices under the same receiver enabling control line. Maximum available current is 10mA.
11. **Carrier Detect**. Pin at high level if the input RF signal level exceeds the set threshold.
12. **Ground.**
14 **Ground.**
17. **Ground.**

18   Data Output. Open collector output to be terminated to the suitable voltage (5mA max drivable current). A typical resistor load would be 10KΩ.

19.   RX Enable. If at high voltage (3 to 5V), the complete receiver is enabled (including Aux Out). If at low voltage (max 0.5V) the receiver is entirely disabled and draws negligible current.

20.   Power Supply.

EXPLANATION NOTES

The following explanation notes refer to a radio system comprising of the **RX-DFM-5V** receiver module and **TX-DFM-5V** transmitter module, operating at 433.85MHz frequency at +40KHz nominal deviation, 10 mW max RF output power on a 50Ω load and 10KHz maximum modulation frequency, corresponding to 19200 baud data stream.

RECEIVER WITH +5V SUPPLY
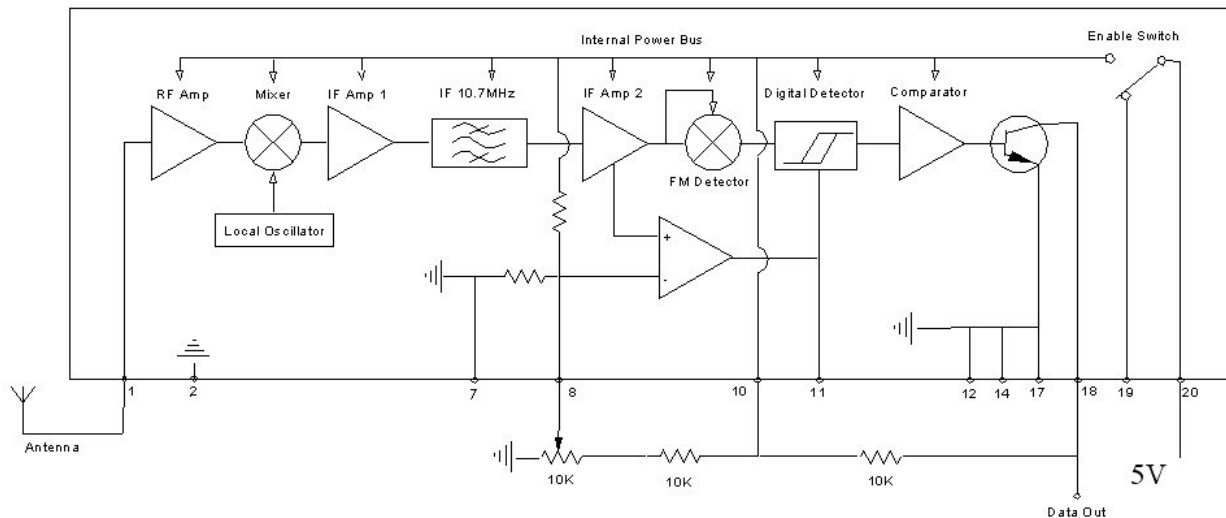
The above diagram shows the receiver connected to a +5V supply. $R_{pull-up}$ is connected to the Aux Out output (pin 10), which is normally enabled only when the receiver is enabled (RX Enable pin = 3 to 5V). With this configuration, the receiver will not draw any supply current, when disabled. This is a useful feature for battery operated systems where battery life can be maximized.

RECEIVER START-UP SEQUENCE
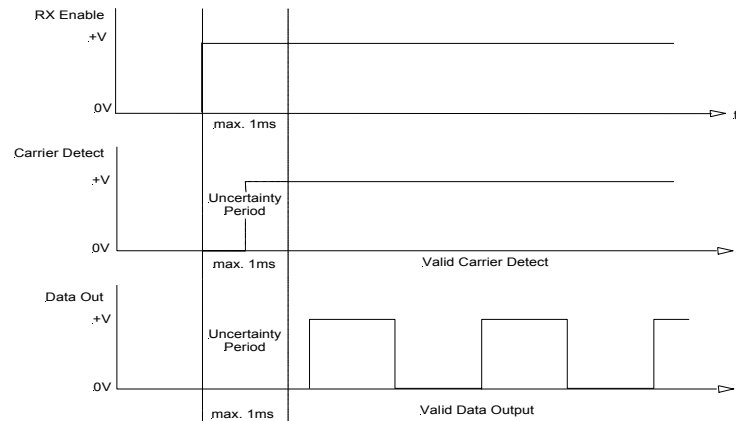
The logic level on pin 19 (RX Enable) defines the receiver's operation. A low voltage (0V) turns the receiver completely off, including the Aux Out output. A high voltage level (3 to 5V) enables the receiver, making it ready to (see above timing charts) correctly receive the transmitted data (the timing charts sequence assumes that a transmitter is already operational and modulating a binary sequence of 0's and1's).

Please note that an short uncertainty time period, no more than 1msec from start-up (Rx Enable ON), is pointed out. During this time both Carrier Detect and Data Output lines may be unreliable.

Since only 1 msec is lost prior to the presence of a valid RF signal, it is possible to implement an external on-off duty cycle power saving circuit to minimize the receivers current consumption and therefore maximize battery life.

SQUELCH LEVEL ADJUSTMENT

With reference to the schematic diagrams, please note the addition of an external potentiometer (10K) connected to adjust the receiver's squelch level.
Digital data output is disabled (0V) for as long as the RF signal level is under a preset reference level.

The correct procedure to adjust the receiver squelch circuitry to obtain the best sensitivity is as follows:

- Make sure that no interfering transmitter is operating on the receiver frequency band. Put the receiver into the normal operating conditions (i.e. Use the final product antenna, apply the right supply voltage, etc.)
- Set the potentiometer to maximum, forcing the top reference level. This position will block out all signals with an RF level below a rather high value. Check that both pin 11 (Carrier Detect) and pin 18 (Data Output) are at a low level.
- Adjust the potentiometer toward minimum, up to the point where digital noise is detected and shown on pin 18: this indicates that the squelch reference voltage is now of the same value as the RF noise from the antenna. This reference level identifies the best sensitivity available from the receiver. It should be better then -100dBm input.
- Slowly adjust the potentiometer again towards maximum voltage, up to a reference level that assures a firm low logic level on both pin 11 and 18.

The receiver will now be operating to detect all those RF signals higher than the squelch preset level. This is higher than the intrinsic system noise and prevents receiving false data out of the receiver, whilst keeping the receiver at maximum sensitivity. If further discrimination between the valid RF signal and

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other interfering signals (of lower magnitude) is necessary, increase the squelch reference level theshold step by step up to a satisfactory level.

The above procedure, although performed without instruments, is safe and yields good results but cannot provide numerical results.

RS232 STANDARD COMPATIBILITY AND 2400 to 19200 BAUD RATE

The receiver's RX Enable input and the Carrier Detect and Data Out outputs are compatible with positive logic ie levels going from 0V to positive voltages: this requires that an interface be used between the receiver itself and any host unit (for example a Personal Computer) to directly handle two RS232 standard inputs and one output.

A recommended interface circuit can be constructed around a MAX232 integrated circuit, with both logic level conversion of the signals out of the receiver (0/5V converted in the corresponding RS232 levels, ie +12/-12V) and the reverse conversion for the input signal (keeping in mind that 3 to 5V is the upper level and less than 0.5V is the low level).

The normal logical level of the receiver data output, when no carrier is present or it is just below squelch threshold, is low (0V) and this is to be considered as a stop bit in the RS232 protocol. A logic inverter is thus required on the input line to a MAX232 I.C.

The following actions describe the sequence in receiving a 10bit byte (1 start bit, 8 data bits, 1 stop bit) of data:

1. Wait for a firm indication from carrier detect, that an adequate RF signal is received.
2. Ignore the data word received during the waiting time, as noise spikes can corrupt it and therefore may be invalid data.
3. Start to receive the complete data string starting from the first following start bit.

Action at point 2. is required due to the possibility that the transient signal during carrier detection could generate a false start bit. This requires that the transmitter must also send out the unmodulated carrier for at least a 2 bytes transmission period, to let the receiving system discard at least one byte without losing any part of the data.

The system does not require any special initialization string or byte to be sent and, in the majority of applications. The above precaution may also not be necessary when the system design assures the best immunity from false signals, particularly when using increased squelch levels.
Please note, that the system has no limitation in the bits combination within any byte; sequences as 00 or FF are processed with no problem and do not require special handling as required on other systems. There is also no limitation in the timing and duration of the transmitted data. The system only requires that any byte is identified by a start bit and ended with a stop bit.

To correctly end the data sequence broadcast and received, follow the procedure:
• Check the Carrier Detector for a valid logic level before accepting a byte as valid data.
• Discard a received data byte if the Carrier is not validated.

Low and high data rate limits (2400 baud, 19.2 Kbaud) are not absolute, but are based on the following considerations:

• Low limit: for best performance, the system should see a sequence of high/low levels at least every 10 msec. The given baud rate low limit is therefore prudential. Lower transmission speeds are acceptable but they down-grade both sensitivity and noise immunity.

- Upper limit: the receiving systems has an internal filter that limits the frequency band passing thru it. Higher speeds are therefore acceptable with strong Rf signals that allow safe detection of the modulating data.

Correct reception of data at high baud rates is also dependant on the RS232 data formatter connected to the host. If software filtering techniques are used, better results can be obtained as compared to hardware systems that simply rely on the start bit's rising edge as the only element to signal the start of operation.

Above comments are based on (but not limited to) the RS232 protocol because of its popularity as the universal standard in terms of a comparison base. The **TX-DFM-5V** and **RX-DFM-5V** system has no usage limit other than the need to receive in a 10msec period at least a low-to-high transition, lasting no less than 50 µsec.

CLOSING CONSIDERATIONS

Data handlig technique described above employs both Carrier Detect and Data Out outputs. Usage of both lines is recommended as it gives better assurance of a correct data transmission. This requires that, in the connection to data processing units such as a Personal Computer, also auxiliary RS232 lines are used and handled by the program. Most programming languages can help to write the appropriate routines. Correct program execution timing, both in transmission and reception, can help to maximize data transfer speed.

If Visual Basic is used, it is suggested that timed event sequence is under control, as it is normally difficult to process close data strings with a reliable time interval between them.